analysis is performed by the harmonic balance approach, thus yielding an efficient and fast computer analysis program. The usefulness and efficiency of the method is demonstrated by a simulation example of a MESFET mixer.

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Single-Stage GaAs Monolithic Feedback Amplifiers

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Abstract—**A theoretical and experimental comparison is made of the performance of GaAs MESFET's with and without negative feedback. The devices are fabricated using a six-step MMIC process, which utilizes polyimide for low-capacitance crossovers and silicon nitride for MIM capacitors. Typical RF performance is 9-dB gain with noise figure less than 4 dB from 100 MHz to 3 GHz. The greatest bandwidth is achieved by incorporating a $3\frac{1}{2}$ turn, low Q inductor, which is connected in series with the feedback resistor and is wrapped around the perimeter of the chip to conserve die area.**

I. Introduction

Negative feedback has been shown to be a viable technique for making wide-band amplifiers with GaAs MESFET's. Ulrich [1] reported a wide-band, hybrid amplifier with a gain of 6.5 dB from 10 MHz to 6 GHz. The amplifier was built with a GaAs FET with a transconductance of ~ 75 mS. Several GaAs monolithic amplifiers using negative feedback have also been reported. Nishiuma *et al.* [2] reported a single-stage monolithic feedback amplifier with 8–10-dB gain and a 2.2-dB noise figure from 50 to 2000 MHz. Archer *et al.* [3] built a two-stage GaAs monolithic amplifier with 24-dB gain, a 3-dB bandwidth to 930 MHz, and a noise figure of 5 dB. Honjo *et al.* [4] reported a two-stage monolithic amplifier with 16-dB gain from 9 MHz to 3.9 GHz and with less than 3-dB noise figure from 90 MHz to 3.9 GHz. The first three-stage, negative feedback GaAs amplifier was reported to have 28-dB gain from 30 MHz to 1.7 GHz [5]. In all of these amplifiers, the amount of feedback was controlled by a resistor between gate and drain.

Higher frequency performance has been achieved by adding inductive elements to negative feedback amplifiers. A minimum gain of 4 dB up to 14 GHz was achieved with negative feedback amplifiers by adding drain and feedback inductors [6] or distributed circuit elements [7]. Terzian *et al.* [8] used a gate, drain, and feedback inductor and achieved 6-dB gain from 1–7 GHz, but the noise figure > 6.5 dB was high. A gain of 6 dB from 0.6–6 GHz was reported by Rigby *et al.* [9] for a one-stage amplifier, which used five inductive elements in a 2.8 mm$\times$1.8 mm die. After careful and detailed modeling, Pavio *et al.* [10] achieved 8-dB gain from 6 to 18 GHz with a feedback amplifier.

The work reported here was undertaken to theoretically and experimentally determine the performance tradeoffs that can be made by monolithically adding resistive and resistance-inductive feedback between the gate and drain of a GaAs MESFET. The predicted and actual performance of a 1-mm-wide GaAs MESFET was compared with that of a similar FET to which feedback was added. The theoretical and experiment results showed that the bandwidth of a resistive feedback amplifier can be increased from less than 2 GHz to over 3 GHz by adding a single, low Q inductor in series with the feedback resistor.

II. Circuit Modeling

The amplifiers were designed using a small-signal MESFET model and COMPACT,[1] a microwave design program. A 1-mm wide FET was selected so that the amplifier would have sufficient gain once the feedback was added. The small-signal model for a 1000-μm-wide GaAs MESFET is shown in Fig. 1. This model was similar to those found in the literature [11]–[13]. The element values were determined from a review of the literature and proper scaling to the 1000-μm width. The FET model was used to predict the gain and noise figure of the FET from 100 Mz to 5 GHz with feedback resistors of various sizes (Fig. 2). The performance of the 1-mm wide FET with no feedback corresponds to the curve with $R_F = \infty$. The predicted gain of the FET was nearly 16 dB at 100 MHz with no feedback but decreased as R_F was decreased. The Fukui equations and the constants k_1 and k_2 reported by Fukui were used to calculate $NF_{\min}$, Γ_{opt}, and R_N [14], [15]. These three parameters were then used to model the noise performance of the FET with and without feedback. The noise figure of the FET was less than 1 dB at 100 MHz and 2.5 dB with $R_F = 150\ \Omega$. The modeling clearly showed that the addition of a few hundred Ω feedback resistor R_F degraded the FET performance.

The addition of feedback, however, had the beneficial effect of reducing the input impedance of the FET and thereby improving

Manuscript received Feb. 17, 1985; revised May 17, 1985

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[1] COMPACT Engineering, Palo Alto, CA.

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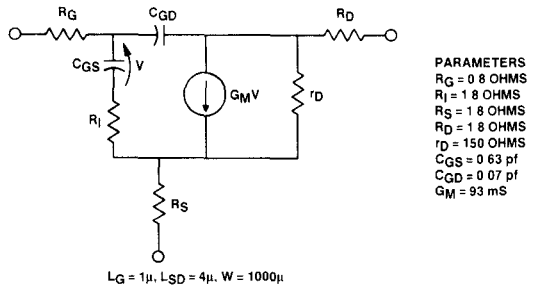

Fig. 1. Small-signal model for 1000-μm-wide GaAs MESFET.

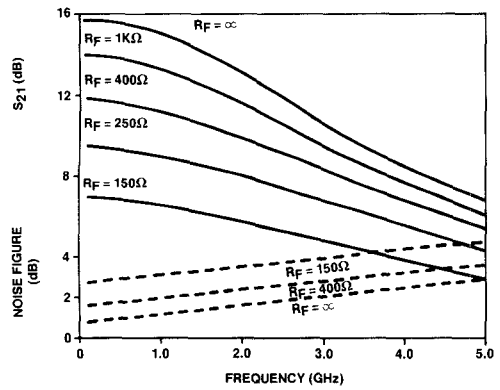

Fig. 2. Predicted gain and noise figure of MESFET with and without feed back.

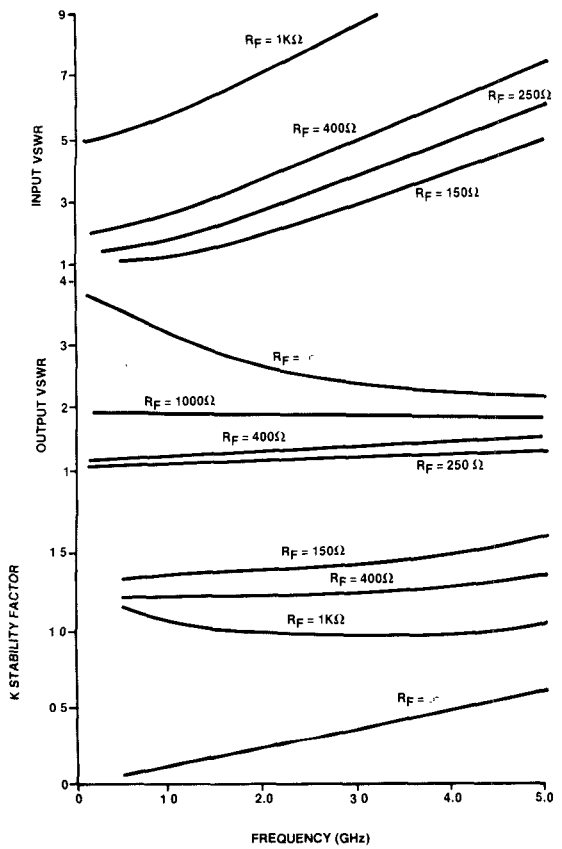

Fig. 3. Predicted input and output VSWR and stability factor K.

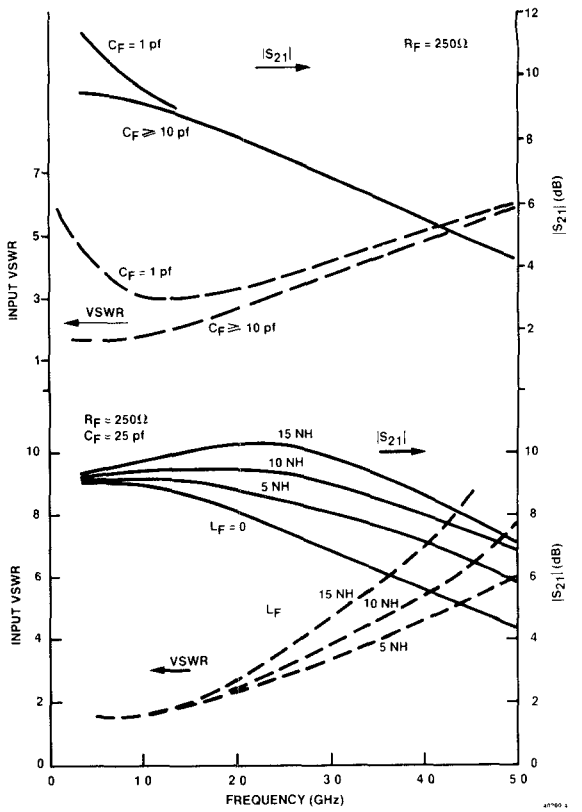

Fig. 4. Predicted gain and input VSWR for different sized capacitors C_F and inductors L_F.

the match between the FET and a 50-Ω system. The input VSWR of the FET was greater than 9:1 with $R_F = \infty$, but less than 5:1 across the 100 MHz to 5-GHz band for $R_F = 150$ Ω (Fig. 3). The output VSWR was also reduced by adding feedback, but not as dramatically. The output impedance of the FET was dominated by r_D (Fig. 1), and therefore was much closer to 50 Ω even with $R_F = \infty$. The stability factor for the 1-mm wide FET was less than one for frequencies from 250 MHz to 5 GHz indicating that the device was not unconditionally stable (Fig. 3). The addition of a feedback resistor made $K \geq 1$ across the entire band.

Although a feedback amplifier could be made by just connecting a resistor from gate to drain, placing a dc blocking capacitor in series with the resistor was helpful from a practical standpoint because with depletion mode MESFET's the drain was biased positively while the gate was biased negatively. An amplifier with a feedback path consisting of a resistor in series with a capacitor is referred to as a RC feedback amplifier. The model predicted that for $C_F \geq 10$ pF the gain and input VSWR were not degraded across the entire bandwidth from 100 MHz to 5 GHz (Fig. 4). For smaller capacitors the input VSWR increased at the low end of the band.

Previous work on resistive feedback amplifiers used a series resistor or a series resistor and capacitor as the feedback path from drain to gate [1]–[5]. Modeling indicated, however, that greater bandwidth could be achieved by inserting an inductor L_F in series with R_F and C_F. The gain and input VSWR versus frequency for several different values of inductance with $R_F = 250$ Ω and $C_F = 25$ pF is shown in Fig. 4. The model predicted that the 1 dB bandwidth could be extended from 2 GHz to 4 GHz by using a 10-nH inductor. The input VSWR was not significantly degraded. This type of amplifier with a series connected resistor,

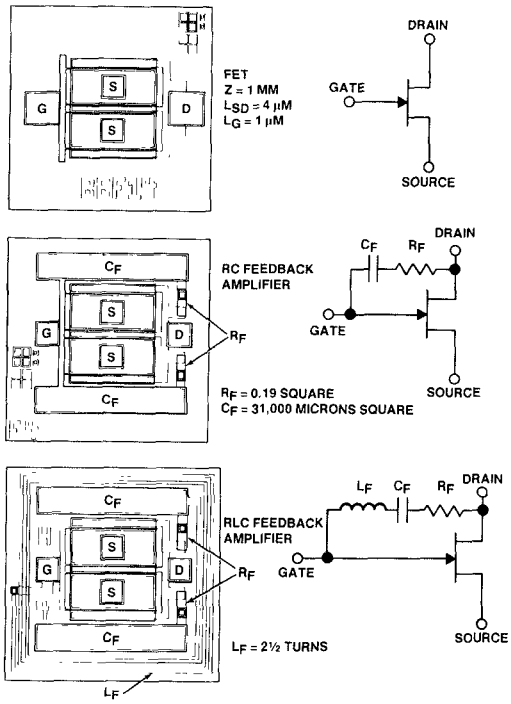

Fig. 5. Layout and circuit schematic of FET, RC amplifier and RLC amplifier.

capacitor, and inductor is referred to as a RLC feedback amplifier.

III. Circuit Layout

The amplifier circuit modeling was useful for determining the optimum circuit element values. However the model gave no information as to circuit layout, which was influenced by numerous factors. In this work the overriding consideration in layout was to make the amplifier as FET-like as possible. This approach appeared to have a number of advantages: small die size, a minimum number of vias and crossovers, and ease of testing in a 70-mil package.

As was mentioned previously a 1-mm wide FET was needed to achieve sufficient gain. The die size was kept small (0.6 mm × 0.6 mm) by going to a multifinger gate design with four 250-μm-wide gate fingers and two source pads for bonding. A photomicrograph of the 1-mm FET is shown at the top of Fig. 5. The standard channel dimensions were a 4-μm source-drain space with a centered 1-μm gate. Some devices were designed with a 6-μm source-drain space in order to determine what effect the larger source-drain spacing had on performance. In addition, other devices were designed with a 2-μm gate length to study what effect the larger gate length had on device performance.

The feedback resistor R_F and dc blocking capacitor C_F were added around the periphery of the 1-mm FET (Fig. 5). To maintain die symmetry the feedback path was divided into two equal paths from gate to drain. In this way the RC feedback amplifier was laid out with only two via holes and no crossovers which were provided by the source bond wires. To keep the process simple, the resistors were designed using the doped GaAs channel material. The capacitors were constructed with first- and second-level metallization with an interposed dielectric. The detailed process flow is given in the next section.

TABLE I
Transistor and Circuit Design Parameters

Device	L_{SD} (μm)	L_G (μm)	R_F (sq.)	C_F (μm)^2	L_F (turns)
FET	4	1	N.A.	N.A.	N.A.
RC Amp	4	1	.38 or .23	62K	N.A.
RLC Amp 2 1/2	4	1	.38 or .23	62K	2 1/2
RLC Amp 3 1/2	4	1	.38 or .23	62K	3 1/2

N A. – Not applicable

The inductor L_F was incorporated in the same die size by wrapping several turns around the perimeter of the chip. In this circuit a low resistance, high Q inductor was not needed because L_F was connected in series with the feedback resistor R_F. The RLC amplifier with a $2\frac{1}{2}$ turn inductor is shown at the bottom of Fig. 5. The design parameters of the FET and amplifiers are summarized in Table I.

IV. Fabrication Process

The first three processing steps were identical to those used to make discrete FET's. The starting material for the process was epitaxial GaAs grown by $AsCl_3$ VPE on semi-insulating GaAs substrate with an interposed high resistivity buffer layer. The doping density of the active layer was 2.5×10^{17} cm^{-3}. The first photolithographic step defined the FET and resistor area (Fig. 6). Mesas were etched with a dilute solution of H_2SO_4 and H_2O_2. The next photolithographic step defined the ohmic contacts for the FET's and epitaxial resistors. After evaporation, the unwanted AuGe/Ni was removed by lift-off. The contacts were alloyed at 450°C for 2.75 min in forming gas. The first half of the process was completed by defining the first-level metal, evaporating TiPtAu (7500 Å), and lifting off the unwanted metal. The first-level metal included gates, interconnects, bottom capacitor plate and square-spiral inductor.

The remainder of the process began by coating the wafer with Dupont PI2545 polyimide and partially curing the 1-μm thick layer. Next, the wafer was coated with positive photoresist, baked, exposed, and developed. The developer removed the exposed resist and proceeded to etch the polyimide under the exposed areas. After the etching was complete, the photoresist was removed in acetone, and the polyimide was cured. As shown in Fig. 6, the polyimide was removed from bonding pads, vias, and the bottom capacitor plate. The capacitor was designed so that the polyimide opening was smaller than the bottom plate so that the perimeter of the bottom plate was covered with polyimide. This was done to increase the capacitor breakdown voltage at the edge of the bottom plate where the top capacitor plate was connected to the rest of the circuit.

Plasma silicon nitride was then deposited on the wafer to a thickness of about 2000 Å. Vias and bond pads were defined using positive photoresist and the exposed silicon nitride was then etched in a CF_4 plasma. The silicon nitride was removed from the bond pads, and vias, but not from the bottom capacitor plate. The process was completed by defining the top capacitor plate and second-level interconnects, evaporating TiAu (9000 Å), and lifting off unwanted metal.

The use of the two dielectrics (polyimide and silicon nitride) solved a number of problems. First, work with low-noise FET's

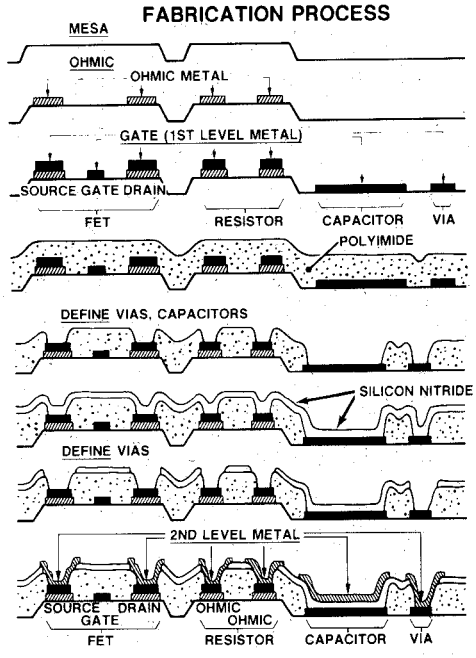

Fig. 6. Circuit fabrication process.

revealed that coating the devices with polyimide did not increase the noise figure, whereas coating them with silicon nitride increased the noise figure significantly [16]. Secondly, the thick polyimide offers a low capacitance at first-level and second-level metal crossovers (0.03 femtofarad/μm^2). This is 11 times smaller than if 2000 Å of silicon nitride were used at crossovers. Third, the polyimide provides increased breakdown strength at capacitor perimeter. The dielectric constant of polyimide is 3.4, whereas that of silicon nitride is 7.4. Therefore silicon nitride offers more capacitance per unit area (327 pF/mm) than if polyimide were used as the capacitor dielectric (30 pF/mm).

A. DC Data

The 1-mm-wide MESFET's fabricated in 750-Ω/square epitaxial GaAs had the following electrical characteristics: $180 \leqslant I_{DSS}$ (mA) $\leqslant 220$, $-3.1 \leqslant V_P$ (v) $\leqslant -2.7$, $80 \leqslant G_M@I_{DSS}$ (mS) $\leqslant 100$, and $75 \leqslant G_M@50$ mA (mS) $\leqslant 85$. The 62,000-μm^2 blocking capacitor C_F had a capacitance of 18 pF for a SiN thickness of 2000 Å. The $2\frac{1}{2}$ and $3\frac{1}{2}$ turns square-spiral inductors had inductances measured at 10 MHz of 8 nH and 14 nH, respectively. The series resistance of the $2\frac{1}{2}$ and $3\frac{1}{2}$ turns inductors fabricated with first-level metallization was 25 and 43 Ω, respectively.

B. RF Data

For RF evaluation the die was bonded in 70-mil, 4-lead FET ceramic packages (ML-7).[2] The RF data was taken with 3 V applied to the drain with the source grounded. The optimum operating point was determined by measuring the gain and noise figure as a function of drain current in a 50-Ω system. This data for the 1-mm wide FET and RLC AMP $3\frac{1}{2}$ is plotted in Fig. 7 as a function of I_{DSS}, which was approximately 200 mA. For both devices the noise figure had a minimum at about 20 percent I_{DSS}. However the minimum was not sharp, and nearly minimum noise figures could be achieved for I_{DSS} between 15 and 30 percent.

[2]Purchased from Kyocera International Inc., San Diego, CA.

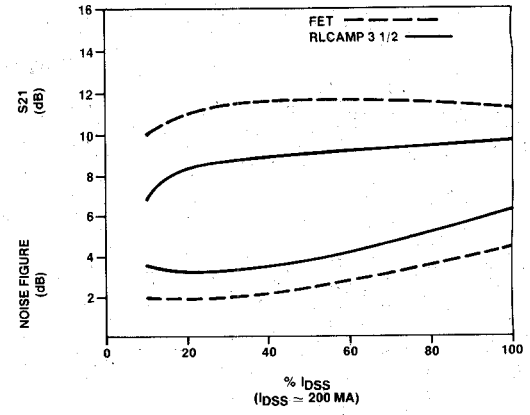

Fig. 7. Measured gain and noise figure versus drain current of FET and RLC AMP $3\frac{1}{2}$ at 1 GHz.

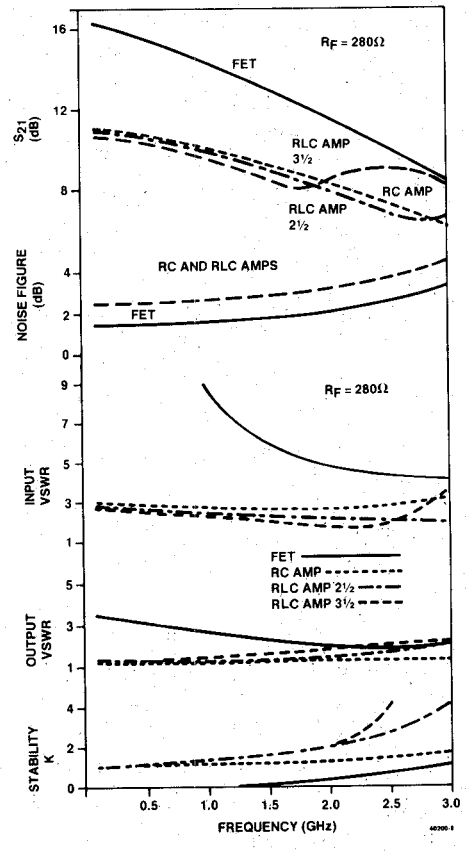

Fig. 8. Gain, noise figure, input and output VSWR, and stability of MESFET and amplifiers.

This agrees qualitatively with the measured and modeled noise figure behavior of low-noise GaAs MESFET's [13]. The gain on the other hand increased monotonically with I_{DSS}, but for currents above 20 percent I_{DSS} the increase was very gradual. The best compromise between high-gain and low-noise figure was achieved for devices biased between 20- and 30-percent I_{DSS}.

The FET and three amplifier designs were characterized from 100 MHz to 3 GHz (Fig. 8). The $|S_{21}|$ of the 1-mm wide FET was 16 dB at 100 MHz and decreased to 8.4 dB at 3 GHz. The addition of the 280-Ω feedback resistor and 18-pF capacitor decreased the gain of the RC AMP to 11 dB at 100 MHz and to 6 dB at 3 GHz. The gain of all the amplifiers was very similar at

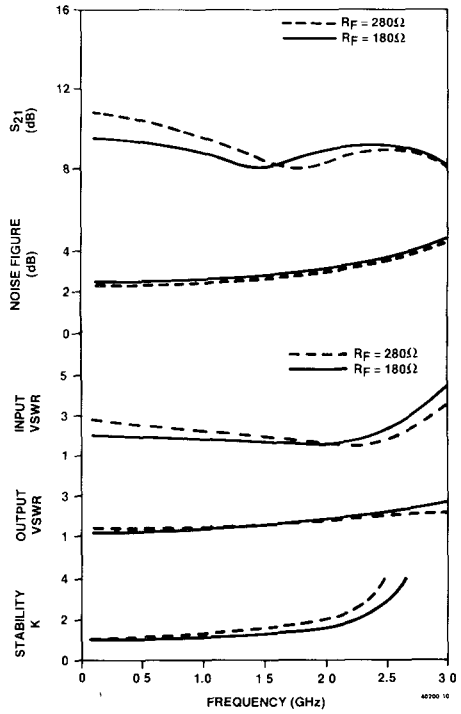

Fig 9. Gain, noise figure, input and output VSWR, and stability of RLC AMP $3\frac{1}{2}$ for $R_F = 180\ \Omega$ or 280 Ω.

low frequencies where the inductor had little effect. The frequency dependent effect of the inductor became evident above 1.5 GHz. The $3\frac{1}{2}$ turn inductor caused a gain increase at about 1.75 GHz and a peak gain of 9 dB at 2.5 GHz. The $2\frac{1}{2}$ turn inductor caused a gain upturn at about 2.75 GHz. Even though the feedback path was a series resonant circuit, the gain increase was not the result of resonance. In fact, the resonant frequency of the $3\frac{1}{2}$ and $2\frac{1}{2}$ turn circuits was 320 and 420 MHz, respectively. The increase in gain was caused by the impedance of the inductor which increased with frequency.

The agreement between the measured and modeled data (Fig. 2) for the FET and RC AMP was rather good. Both the measured and modeled data show that the inductor increased the bandwidth of the amplifier, but the shape of the modeled and measured gain curves were significantly different. Improved agreement was achieved by incorporating the parasitic capacitances, which existed between the turns of the inductor and between the capacitors and inductor. The measured noise figure of the FET and amplifiers is also shown in Fig. 8. Incorporation of the feedback resistor in the amplifier raised the noise figure about 1 dB above that of the FET across the entire band from 100 MHz to 3 GHz. The modeled noise figure was lower than the measured noise figure, but the incremental increase caused by $R_F = 280\ \Omega$ was about 1 dB for both modeled and measured results.

The measured input and output VSWR, and stability factor K are also plotted in Fig. 8. The input VSWR of the FET was significantly higher than that of the FET with feedback especially at the low end of the band. The input VSWR of RLC AMP $3\frac{1}{2}$ increased at the high end of the band as the impedance of the inductor increased. As mentioned previously, the output impedance of the FET and AMP's was dominated by the output resistance r_D of the FET, which was typically several hundred ohms. The data clearly show that the feedback reduced the output VSWR at the low end of the band and to a lesser extent at the upper end of the band. The FET was not unconditionally stable across the entire band as indicated by $K < 1$. However, all three amplifiers had $K \geq 1$ across the entire band which indicated unconditional stability.

The effect of the feedback resistor R_F on the performance of the $3\frac{1}{2}$ turn RLC amplifier is shown in Fig. 9. At 100 MHz, the amplifier with $R_F = 180\ \Omega$ had lower gain, as would be expected. Above 1.5 GHz the two amplifiers have similar performance. As a result the amplifier with $R_F = 180\ \Omega$ had a flatter gain response. The noise figure of both amplifiers was nearly the same. The noise figure data was consistent with the gain data in that for $R_F = 180\ \Omega$ the gain was lower and the noise figure was higher. The input and output VSWR were similar for both amplifiers, but a lower input VSWR at 100 MHz was achieved with $R_F = 180\ \Omega$. Both amplifiers were also unconditionally stable from 100 MHz to 3 GHz.

Amplifiers were also fabricated using FET's with different channel and gate dimensions. In general, as the source-drain spacing and gate length were reduced, performance improved at the expense of circuit yield. All of the previously presented data was for amplifiers wherein the FET-channel dimensions were $L_{SD} = 4\ \mu$m and $L_G = 1\ \mu$m. Increasing the FET source-drain spacing to 6 μm reduced the amplifier gain about 1 dB and raised the noise figure about 0.5 dB across the band from 100 MHz to 3 GHz. Input and output VSWR increased only slightly. Increasing the FET gate length to 2 μm also increased the noise figure about 0.5 dB and decreased the gain about 1 dB. In addition, the amplifier with $L_G = 2\ \mu$m had less bandwidth because C_{GS} (Fig. 1) was larger. Moreover the effect of these two changes was additive. An amplifier with $L_G = 2\ \mu$m and $L_{SD} = 6\ \mu$m had 2 dB less gain and 1 dB higher noise figure.

V. Summary

The performance of 1-mm wide GaAs MESFET's with and without negative feedback was compared experimentally and theoretically. The devices were fabricated using a six-step process which utilized polyimide for low-capacitance crossovers and plasma silicon nitride for high capacitance per unit area capacitors. A good compromise between low-noise figure and high gain was achieved by operating the amplifiers at 20-percent I_{DSS}. Typical measured performance was 9-dB gain with noise figure ≤ 4 dB from 100 MHz to 3 GHz with input VSWR ≤ 3, output VSWR ≤ 2 and $K \geq 1$. The greatest bandwidth was measured on amplifiers which incorporated a $3\frac{1}{2}$ turn, low Q inductor in series with the feedback resistor. Gain flatness was improved by reducing R_F to 180 Ω.

Acknowledgment

The authors wish to thank members of the III-V group at Motorola for their encouragement and support and especially M. Scott for typing the manuscript after innumerable revisions.

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Homodyne and Heterodyne Studies of GaAs and InP Millimeter-Wave GUNN Mixers

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Abstract—**Detailed investigations of both homodyne and heterodyne self-oscillating mixers have been conducted. The active devices were GaAs and InP Gunn diodes, operating in the frequency region of 94 GHz. In addition to the fourfold comparisons of GaAs and InP homogyne and heterodyne mixers, finer comparisons were made with recently developed diode structures. The InP diodes were of two types: either n^+-n-n^+ sandwich, or n-n^+ with a current-limiting cathode contact. The GaAs diodes were of n^+-n-n^+ sandwich structure.**

Sensitivity of −80 dBm (homodyne) at a few hundred hertz beat frequency was obtained with InP n^+-n-n^+ diodes. These results were of the order of 6 dB better than those with GaAs n^+-n-n^+ and InP n-n^+ diodes. With heterodyne, the InP n^+-n-n^+ gave sensitivity approaching −90 dBm with intermediate frequency at 70 MHz and an IF bandwidth of 33 MHz, which constituted a superiority of 10 dB over the other two diode types.

I. Introduction

Interest in millimeter-wave self-oscillating mixers has been on the increase in recent years [1]–[5] mainly because of the high burn-out power limit, ruggedness, low cost, and comparatively simple circuitry for signal processing. Moreover, the advent of high-frequency GaAs and InP Gunn diodes has brought considerable innovation to the materials technologies and device structures in order to meet the requirements of efficiency and high powers for millimeter-wave generation using solid-state devices [6], [7].

It is, therefore, the main purpose of this paper to report a comparative study of some of the new device features in homodyne and heterodyne self-oscillating mixers around 94 GHz, since it is to be ascertained whether reasonable performances could be achieved with these recent devices.

II. Gunn Device Characteristics

The GaAs Gunn diodes were made by the vapor-phase epitaxy (VPE) technique using arsenic trichloride, and consisted of three-layer structures: n^+-n-n^+ with integral heat sink. The active region presented a carrier density of 7×10^{15} to 1.2×10^{16} atoms cm^{-3} with an active distance between 2.0 and 3.0 μm. The total GaAs thickness was 10 to 12μm, and a Ni/Ge/Au metal scheme was used to provide the ohmic contacts, with specific resistance within 1 to $3\times10^{-6}\cdot cm^2$ [6], [9].

Measurements carried out of power and conversion efficiency showed that the devices used in the experiments delivered typically 12 mW at about 1 percent efficiency at 94 GHz.

The InP Gunn diodes were of two types: 1) a two-layer structure of n-n^+ with a current limiting cathode contact, and 2) a three-layer structure of n^+-n-n^+. Both types of InP diodes were also fabricated by the VPE process, using phosphorous trichloride, indium, and hydrogen. They were of the integral heat-sink-type. The active regions had carrier concentration of 6 to 8×10^{15} atoms cm^{-3} with active layer thicknesses from 1.5 to 2.5 μm. The total InP thickness was of the order of 20 μm for the InP n-n^+ devices. Contacts for the InP were of a similar metal scheme to those described for the GaAs diodes [10]. The main difference between the two types of InP devices was the presence of a current-limiting cathode contact which controls the injection of carriers into the active layer. The $I-V$ characteristics of the InP n-n^+ devices do not present the familiar drop-back in bias current above threshold. Actually, the bias current increases with voltage due to self heating of the diodes [11].

Evidence is presently being accumulated to establish the function of nonohmic contacts in improving the efficiency of operation of InP devices at higher frequencies. However, for lower frequencies, it is well established that the use of such types of contacts will limit the device average current density to an optimum value. When optimized, the reverse-bias saturation current density at the cathode is slightly greater than that of the saturated drift velocity region of the device. Although this is a necessary condition to improve efficiency, a sufficient condition is that current density at the cathode varies only slightly with the electric field at the cathode [11]–[17].

Measurements carried out showed that the InP n-n^+ diodes used in the experiments delivered typically 25 mW at about 4-percent efficiency at 94 GHz. The InP n^+-n-n^+ devices yielded output powers of the order of 15 mW with conversion efficiency typically around 1.5 percent. Both GaAs and InP diodes were packaged in pico-pill capsules resisting on round flanges on top of threaded studs.

III. W-Band Oscillator–Mixer Hardware Configurations

One of the basic advantages of the self-oscillating mixer is the fact that it does not need a separate local oscillator (LO) and mixer diode. It acts simultaneously as an LO and a mixing element because nonlinearities are always present in such a

Manuscript received February 11, 1985; revised June 24, 1985. This work was supported in part by the SERC, United Kingdom, and by the Ministry of the Navy, Brazil.

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0018-9480/85/1100-1249$01.00 ©1985 IEEE